

ABSTRACT OF THE DISCLOSURE

A 40-Gb/s clock and data recovery (CDR) circuit incorporates a quarter-rate phase detector and a multi-phase voltage controlled oscillator to re-time and de-multiplex a 40-Gb/s input data signal into four 10-Gb/s output data signals. The circuit is fabricated
5 in 0.18 μm CMOS technology.

"Express Mail" mailing label number EV 329956135US
Date of Deposit JULY 1 2003
I hereby certify that this paper or fee is being de-
posited with the United States Postal Service "Express Mail"
Post Office to Addressee" service under 37 CFR 1.10 on
the date indicated above and is addressed to:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
Suzie Mccleave
(Printed name)
AJ
(Signature)